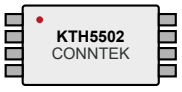
KTH5502

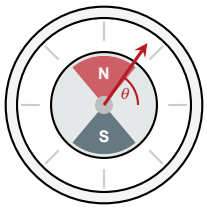
3D Hall Magnetic Angle Sensor

High-Precision 3D Hall Magnetic Angle Sensor



SOP-8L

DFN-8L



Motor Angle Detection

Typical Applications

- BLDC Motor Control
- Robot Joints
- Gimbal Stabilizers
- Joysticks / Gamepads
- Smart Knobs

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Rev. 1.3

DS-KTH5502-001

Contents

1 Overview

The KTH5502 is a high-precision absolute angle sensor IC based on vertical Hall technology, supporting full-angle (0–360°) measurement. The chip integrates vertical Hall elements on the X and Y axes and a horizontal Hall element on the Z axis, enabling simultaneous detection of magnetic field variations in all three directions.

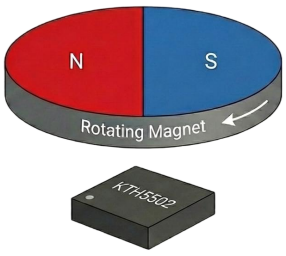
Benefiting from the excellent orthogonal matching characteristics, low offset design, and high-performance signal chain of vertical Hall technology, the KTH5502 converts magnetic signals into digital signals through a high-precision amplification circuit and a 16-bit ADC, combined with dedicated algorithm processing to achieve high-resolution absolute angle output in the XY plane.

2 Features

- High-precision vertical Hall technology, supporting full-angle (0–360°) measurement
- 16-bit resolution absolute angle output
- Wide operating voltage: 1.7V ~ 3.6V
- Wide temperature range: -40°C ~ +125°C
- Low power consumption: typical operating current 4–6mA
- Rich interfaces: I²C, SPI, AB quadrature encoding, PWM, analog voltage
- Maximum supported speed: 5000 RPM
- AB quadrature output up to 1024 lines/rev
- Available in SOP-8L and DFN2×2-8L packages

3 Applications

- Absolute angular position detection
- BLDC / stepper / gimbal motor control
- Robot joint motors
- Industrial knobs and control panels
- Joysticks and game controllers
- Steering angle sensors
- Valve position detection
- Replacement for traditional optical encoders



4 Device Information

4.1 Model Classification and Selection

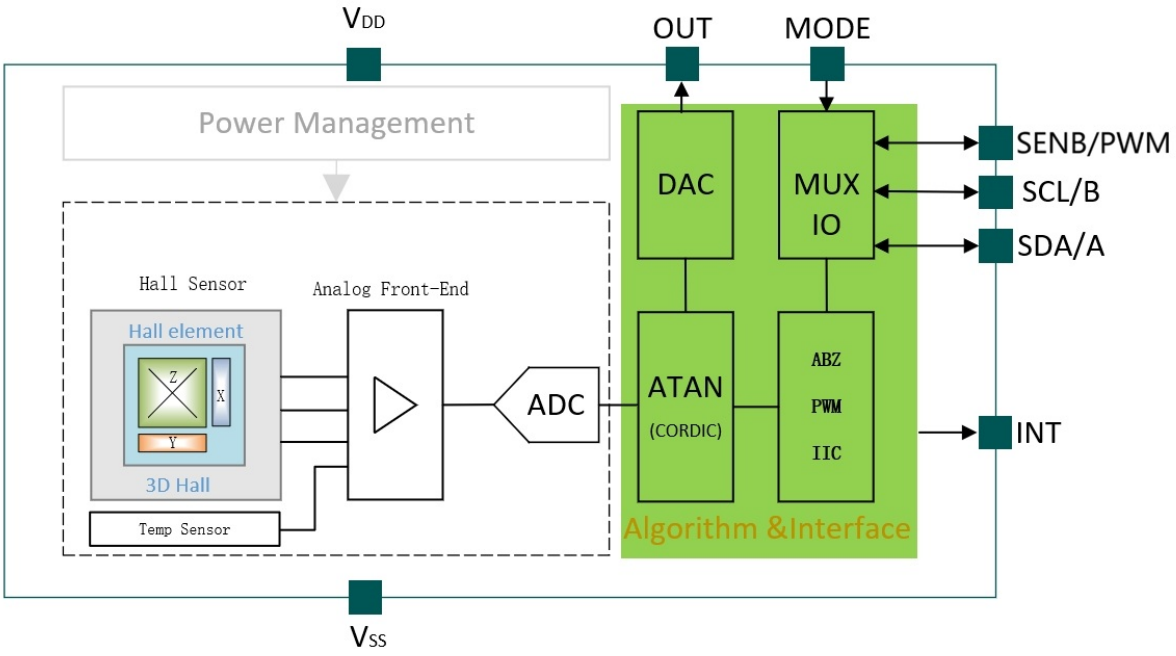
By ordering part number, the KTH5502 is divided into **Base Model** and **Standard Line Count Model** categories (naming consistent with Chapter 15 Ordering Information). The main differences lie in the function of pin 3 (OUT/A0), whether the I²C slave address is configurable via A0, and whether analog voltage output is available. Both model types support AB quadrature encoding, PWM, I²C, or SPI interfaces via the MODE pin selection, but wiring must be verified against the selected part number to avoid incorrectly connecting the A0 pin of a base model as an analog output load.

Feature	Base Model	Std. Line Count Model
AB quadrature output (MODE=Low)	Supported	Supported
PWM output	Supported	Supported
I²C / SPI (MODE=High)	Supported	Supported
Analog voltage output (OUT pin)	Not supported (OUT/A0 used as I²C address pin A0)	Supported
I²C 7-bit slave address	A0 to GND: 0x6A; A0 to VDD: 0x6B	Fixed 0x6A
Line count / ordering suffix	Fixed 12 lines; see 15.1	With AB line count and/or analog suffix; see 15.1

4.2 Device and Package Overview

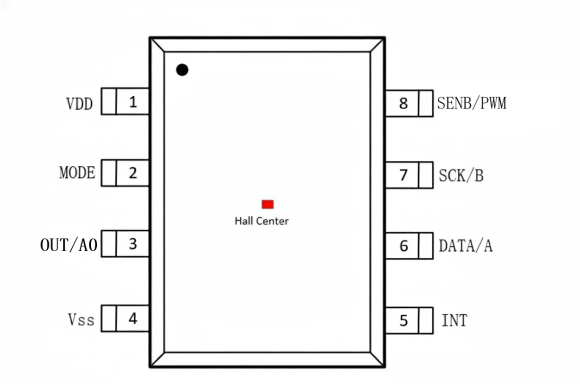
Part Number	Package	Package Size (Nominal)
KTH5502	SOP-8L	5.00mm × 4.00mm
KTH5502	DFN-8L	2.00mm × 2.00mm

5 Functional Block Diagram

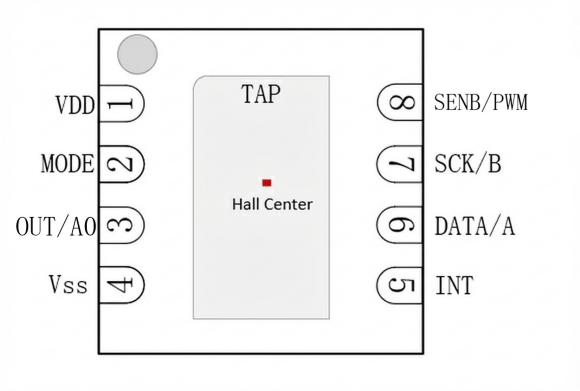


6 Pin Configuration & Description

6.1 Package Pinout Diagrams



SOP-8L Package Pinout



DFN-8L Package Pinout

Note: The red frame in the pinout diagram indicates the 3D Hall sensing center point, located at the geometric center of the package.

6.2 Pin Function Description

Pin	Name	Description
1	VDD	Positive supply voltage, operating range 1.7V ∼ 3.6V
2	MODE	Operating mode selection. Low: AB quadrature output; High: I²C (SPI) interface. Built-in 200kΩ pull-up resistor
3	OUT/A0	**Base Model:** Used as I²C address selection pin A0; 7-bit address is 0x6A when A0 is tied to GND (low), 0x6B when tied to VDD (high). **Std. Line Count Model:** Used as analog voltage output; I²C 7-bit address is fixed at 0x6A.
4	GND	Ground
5	INT	Measurement complete indicator, interrupt output
6	DATA/A	I²C data line SDA / SPI data line DATA / Incremental signal A
7	SCK/B	I²C clock line SCL / SPI clock line SCLK / Incremental signal B
8	SENB/PWM	I²C/SPI chip select (high: I²C mode) / PWM output

7 Absolute Maximum Ratings

WARNING: Exceeding the absolute maximum ratings may cause permanent damage to the device. Long-term operation under extreme conditions may affect device reliability.

Parameter	Symbol	Min	Max	Unit
VDD pin voltage	V_{DD}	-0.5	4.0	V
Operating temperature	T_A	-40	+125	°C
Storage temperature	T_{STG}	-55	+150	°C
ESD (HBM)	V_{ESD}	—	±5.0	kV
ESD (CDM)	V_{ESD}	—	±1.0	kV

8 Electrical Characteristics

Test conditions: V_{DD} = 3.3V, T_A = 25°C, unless otherwise noted.

8.1 Power Supply Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	1.7	3.3	3.6	V
Operating current	I_{DD}	VDD=3.3V	4	—	6	mA
Power-on time	T_{PwrUp}	VDD ramp	—	—	20	ms
System delay	T_{Delay}	AB quadrature output mode	—	100	—	μs

8.2 Angular Measurement Performance

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Angle resolution (digital mode)	Res_θ	I²C/SPI	—	16	—	bits
Integral non-linearity	INL	B=50mT	—	±1.0	±2	°
Differential non-linearity (AB output)	DNL	AB quadrature output	—	±0.2	—	°
Transition noise (AB output)	T_N	Static measurement	—	0.1	—	°rms
Rotation speed	R_S	Continuous rotation	—	—	5000	RPM

8.3 PWM Output Parameters

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PWM frequency	F_{PWM}	pwmFreq=0 (default) / pwmFreq=1	-5%	972/486	+5%	Hz
PWM output resolution	Res_{PWM}	pwmFreq=0 (default) / pwmFreq=1	—	13/14	—	bits
Rise time	T_{Rise}	CL=1nF, 10%-90%	—	—	1	μs
Fall time	T_{Fall}	CL=1nF, 90%-10%	—	—	1	μs

8.4 Digital I/O Parameters

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input logic high voltage	V_{IH}	—	0.7×V_{DD}	—	—	V
Input logic low voltage	V_{IL}	—	—	—	0.3×V_{DD}	V
Output logic high voltage	V_{OH}	I_{load}=1mA	V_{DD}-0.5	—	—	V
Output logic low voltage	V_{OL}	I_{load}=1mA	—	—	0.5	V
Rise time	T_{RISE}	CL=100pF	—	—	20	ns
Fall time	T_{FALL}	CL=100pF	—	—	20	ns

9 Digital Communication Interface

The KTH5502 supports I²C/SPI digital communication interfaces. The I²C 7-bit slave address for the standard line count model is 0x6A; for the base model, the address is selected by pin A0 (OUT/A0): 0x6A when A0 is tied to GND, and 0x6B when tied to VDD. Measurement data readback includes CRC (Cyclic Redundancy Check) functionality for improved data reliability.

9.1 Command Format Description

Operation	Write Cmd	Write Data 1	Write Data 2	Write Data 3	Read Data 1	Read Data 2	Read Data 3	CRC
Write Register	0x60	REG[15:8]	REG[7:0]	REG_ADDR«2	Status	—	—	—
Read Register	0x50	REG_ADDR«2	—	—	Status	REG[15:8]	REG[7:0]	—
CM Continuous Measurement	0x16	—	—	—	Status	—	—	—
EX Exit Measurement	0x80	—	—	—	Status	—	—	—
RM Read Measurement	0x4X	—	—	—	Status	Data (defined by X)		CRC[7:0]

RM command X field definition: $X[3{:}0] = \{b_1, b_0, 0, 0\}$, corresponding to {magnXYplane, AngleXYplane, reserve, reserve} —two 16-bit measurement items. Each bit set to 1 returns 2 bytes of data in the fixed order: `AngleXYplane[15:8]` → `AngleXYplane[7:0]` → `magnXYplane[15:8]` → `magnXYplane[7:0]`; deselected items are omitted from the sequence. AngleXYplane refers to the angle in the corresponding plane, and magnXYplane refers to the magnetic field strength in that plane.

Example: The host sends 0x4C (X=1100). The chip returns the frame: `Status` → `AngleXYplane[15:8]` → `AngleXYplane[7:0]` → `magnXYplane[15:8]` → `magnXYplane[7:0]` → `CRC[7:0]`.

Note: The above commands apply to both I²C and SPI. Readback data is a 16-bit unsigned value; the number of readback bytes depends on the command configuration, ranging from 2 to 4 bytes. CRC uses the CRC8/ITU method; only the RM read measurement command supports CRC. During CRC calculation, deselected channels are padded with zeros.

9.2 CM Continuous Measurement Mode

After the host sends the CM continuous measurement command, the chip continuously measures the XY plane angle until the host sends an idle mode command.

For example, when the host sends command 0x16, the chip enters CM continuous measurement mode and continuously measures the angle in the XY plane.

CM Mode Measurement Frequency Configuration:

The measurement frequency in CM mode is controlled by the `CM_measTime[9:0]` bits of the Digital Filter and CM Mode Configuration Register `DIG_FLT` (address: 0x1C). For detailed configuration, refer to Section 11.6 ”Digital Filter and CM Mode Configuration Register DIG_FLT”.

9.3 Idle Mode

After the host sends the idle mode command, the chip enters the idle state. While the chip is in CM measurement mode, no operations other than measurement data readback are allowed (e.g., register read/write). To perform other operations, the idle mode command must be sent first.

Note: The Idle state refers to when the chip is not in measurement mode. The Standby state refers to when the chip is in measurement mode but idle between measurements. When exiting measurement mode via the idle command, wait one full measurement cycle before performing other operations.

9.4 Data Read Frame

After the chip completes a measurement, the Data Read Frame can be used to read the chip’s operating status (Status) and all magnetic field-related measurement data in a single transaction.

When the host sends a Data Read Frame, it can choose to read angle or magnetic field data. All data is returned as 16-bit unsigned values.

9.5 Register Read/Write

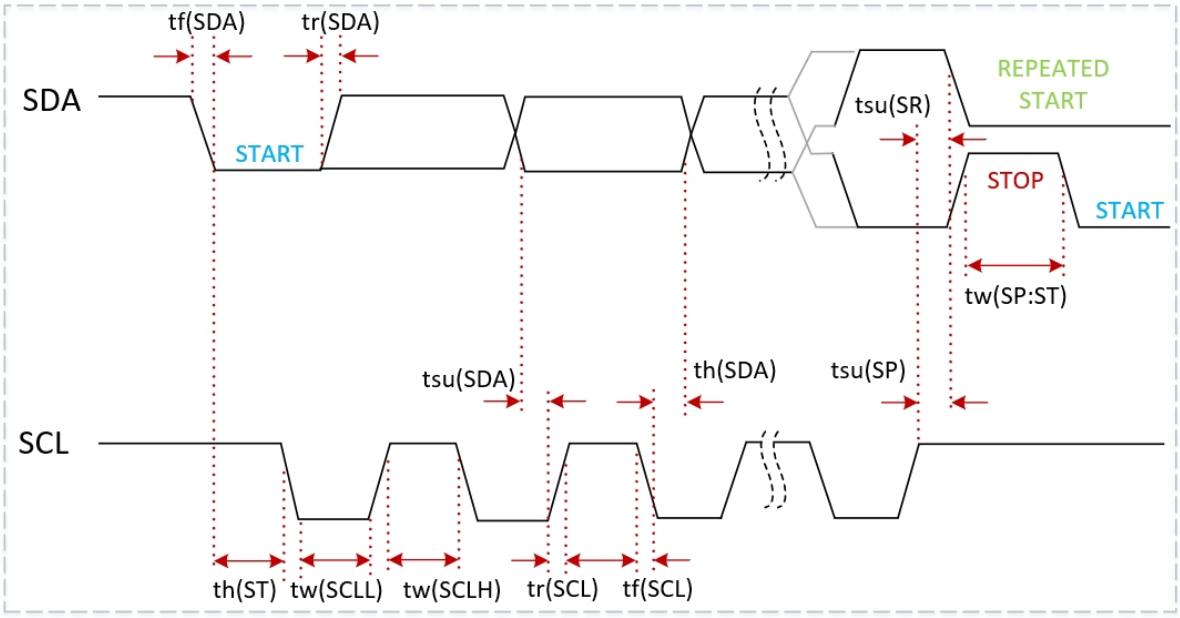
The chip automatically performs internal initialization after power-on. After the power supply stabilizes, the chip loads OTP values into the corresponding registers within 4 ms. Communication with the chip is prohibited during this period (within 4 ms after power-on).

After initialization is complete, the chip enters the Idle state, allowing communication and measurement operations. When reading or writing registers, the register address should be left-shifted by two bits.

9.6 I²C Communication Mode

The following parameters are measured at room temperature (25°C) and V_{DD} = 3.3V.

Parameter	Description	Std Min	Std Max	Fast Min	Fast Max	Unit
f(SCL)	SCL clock frequency	—	100	—	400	kHz
tw(SCLL)	SCL clock low time	4.7	—	1.3	—	μs
tw(SCLH)	SCL clock high time	4	—	0.6	—	μs
tsu(SDA)	SDA setup time	250	—	100	—	ns
th(SDA)	SDA hold time	—	3.45	—	0.9	μs
tr	SDA and SCL rise time	—	1000	—	300	ns
tf	SDA and SCL fall time	—	300	—	300	ns
th(ST)	START condition hold time	4	—	0.6	—	μs
tsu(SP)	STOP condition setup time	4	—	0.6	—	μs



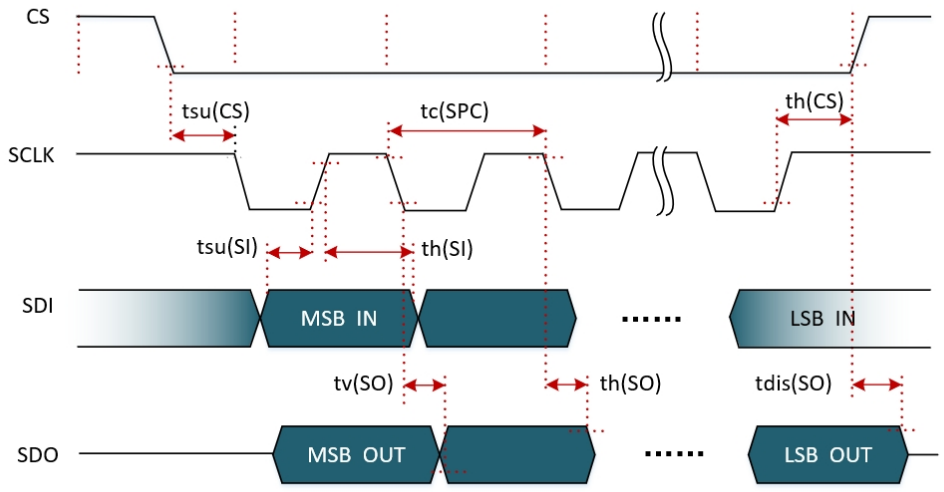
9.7 SPI Communication Mode

SPI uses a 3-wire interface, Mode 3: CPHA=1 (data changes on the first edge, sampled on the second edge), CPOL=1 (high level is the idle state).

The following parameters are measured at room temperature (25°C) and V_{DD} = 3.3V.

Parameter	Description	Min	Max	Unit
tc(SPC)	SPI clock period	200	—	ns
f(SPC)	SPI clock frequency	—	5	MHz
tsu(CS)	CS setup time	5	—	ns
th(CS)	CS hold time	10	—	ns
tsu(SI)	SDI input setup time	5	—	ns
th(SI)	SDI input hold time	15	—	ns
tv(SO)	SDO valid output time	—	50	ns
th(SO)	SDO output hold time	5	—	ns
tdis(SO)	SDO output disable time	—	50	ns

Note: SDI and SDO are internal chip signals accessed through the DATA pin.



10 Output Modes

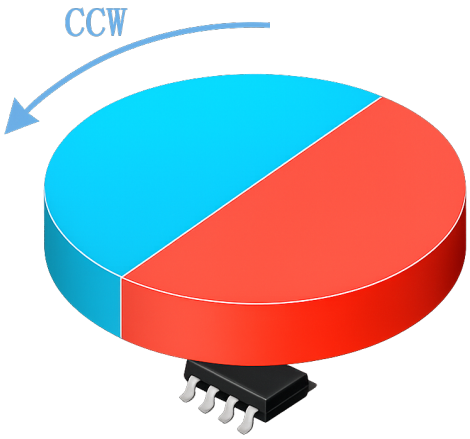
The KTH5502 supports multiple output modes, including AB quadrature encoding, analog voltage output, and PWM (Pulse Width Modulation) output.

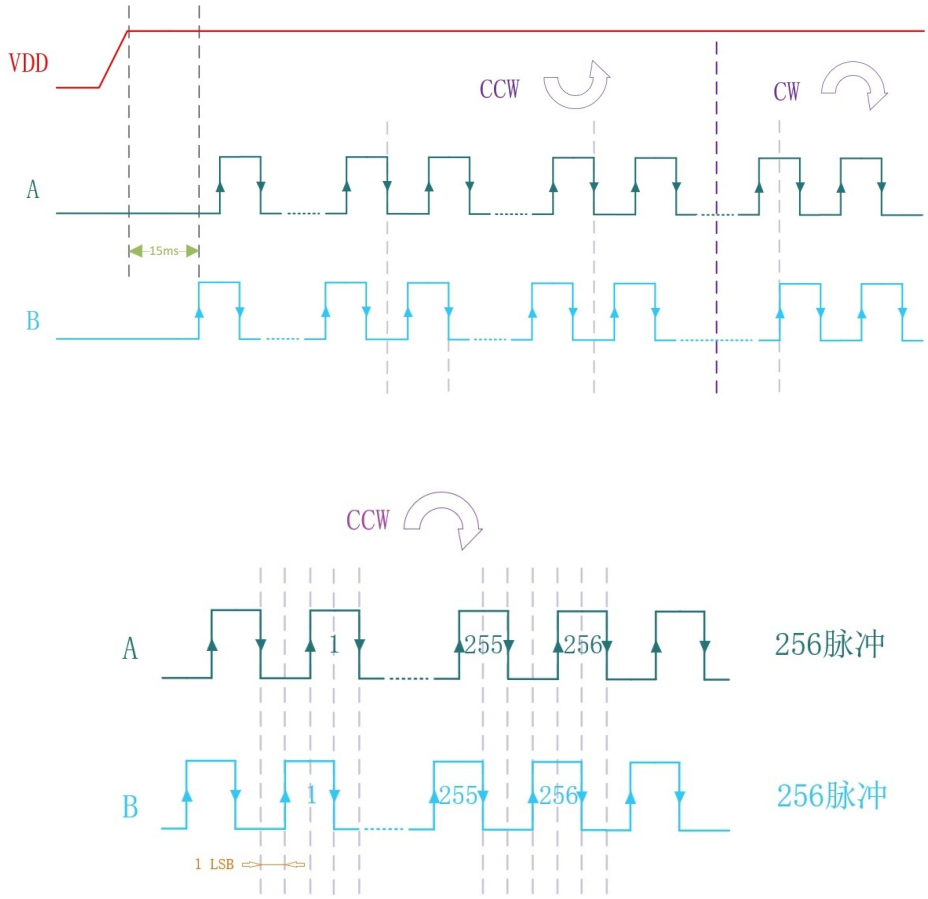
Default Configuration	Value
Output mode	Selected by MODE pin level
PWM frequency (pwmFreq)	972 Hz / 13 bit (pwmFreq=0)

10.1 AB Quadrature Encoding Output Mode

The AB quadrature encoding output mode provides two quadrature signals: Phase A and Phase B. **Direction is defined from the top view of the chip**. If viewed from the magnet or mechanism side, the CW/CCW and A/B phase lead relationship will be opposite to the description in this document. Phase A and Phase B signals have a 90° phase difference. When the magnet is above the chip and rotates counterclockwise (CCW), the rising edge of Phase B leads Phase A by 90°. Conversely, when rotating clockwise (CW), the rising edge of Phase A leads Phase B by 90°.

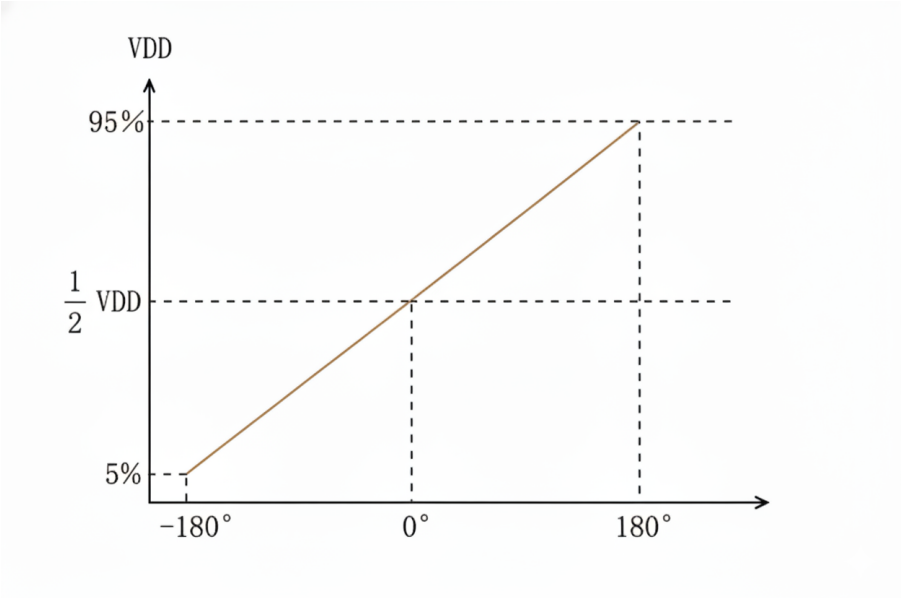
- Phase A and Phase B signal frequency is proportional to rotation speed
- Output signals are push-pull, with levels of 0V/VDD
- Supports programmable resolution settings (12–1024 lines)





10.2 Analog Output Mode

The analog output mode provides an analog voltage output linearly proportional to the angular position. The midpoint is $V_{DD}/2$: when the angle is 0°, the OUT pin outputs $V_{DD}/2$. The typical analog output range is 0.05×V_{DD} ~ 0.95×V_{DD}, corresponding to an angle range of $-180° \sim +180°$.



10.3 PWM Output Mode

The PWM output mode provides a pulse width modulated signal where the high pulse duration is proportional to the angular position. t_{ON} and t_{OFF} are the high-level and low-level durations within a single PWM cycle respectively (see figure below). The angle Ang (unit: °) is derived from the pulse width as:

For `pwmFreq=0` (13-bit, default):

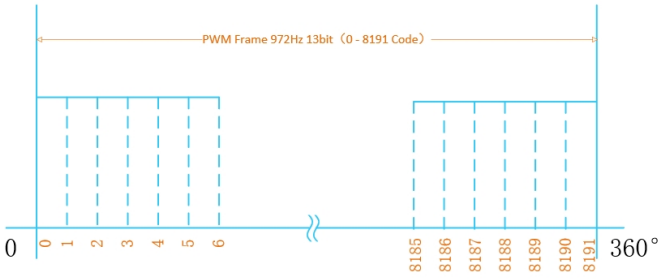
$$Ang = \frac{360}{8192}\left(\frac{(8192+32)\cdot t_{ON}}{t_{ON}+t_{OFF}} - 16\right) \tag{1}$$

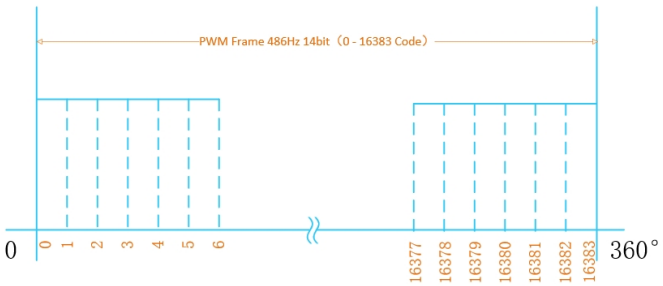
For `pwmFreq=1` (14-bit):

$$Ang = \frac{360}{16384}\left(\frac{(16384+64)\cdot t_{ON}}{t_{ON}+t_{OFF}} - 32\right) \tag{2}$$

where $8192 = 2^{13}$ and $16384 = 2^{14}$ are the full-scale angular resolution counts; $(8192+32) = 8224$ and $(16384+64) = 16448$ are the total PWM cycle counts, consistent with the chip's internal angle quantization.

PWM output is suitable for long-distance transmission applications. Frequency selection is configured via the pwmFreq bit (bit 13) of the OSR_CFG (0x19) register.





11 Register Map

11.1 Register Overview

Address	Name	R/W	Description
0x06	STATUS	R	Status register
0x19	OSR_CFG	R/W	ADC oversampling rate configuration register
0x1A	ANG_ZERO_L	R/W	Angle zero trim low byte register (forms 16-bit angle zero parameter with OUT_TRIM)
0x1B	OUT_TRIM	R/W	Analog output trim register (gain/offset)
0x1C	DIG_FLT	R/W	Digital filter and CM mode configuration register

11.2 Status Register STATUS (Address: 0x06)

Bit Name	Bit	R/W	Description
Roll_cnt	3:0	R	Counter increments automatically each time the chip completes a full measurement set requested by the host. Wraps to zero when the maximum value is reached
Failing	4	R	Set to 1 when the current command is invalid
RESERVED	6:5	R	Reserved bits
CM	7	R	Set to 1 when the chip enters CM measurement mode

11.3 ADC Oversampling Rate Configuration Register OSR_CFG (Address: 0x19)

Bit Name	Bit	R/W	Default	Description
RESERVED	12:0	RO	0x109D	Factory-internal configuration; user modification not allowed
pwmFreq	13	RW	0	PWM frequency selection: 0 = 972 Hz (13-bit), 1 = 486 Hz (14-bit)
magnOsr	15:14	RW	2’b00	Magnetic field measurement ADC oversampling rate. Encoding: 2’b00 = 128, 2’b01 = 32, 2’b10 = 64, 2’b11 = 256

11.4 Angle Zero Trim Low Byte Register ANG_ZERO_L (Address: 0x1A)

Bit Name	Bit	R/W	Default	Description
angle_zero	7:0	RW	0x00	Lower 8 bits of the angle zero trim parameter; forms a 16-bit angle zero trim parameter with OUT_TRIM[7:0]
RESERVED	15:8	RW	0xXX	Reserved bits. Recommended: read current value before writing, modify only `angle_zero[7:0]`, then write back

Angle Zero Trim Parameter:
The lower 8 bits of register `ANG_ZERO_L` (0x1A) and the lower 8 bits `out_offset[7:0]` of register `OUT_TRIM` (0x1B) together form a 16-bit angle zero trim parameter. This parameter applies to both angle output and PWM output, but not to analog output.
Angle zero trim parameter = {`OUT_TRIM[7:0]`, `ANG_ZERO_L[7:0]`}, where `OUT_TRIM[7:0]` is the upper 8 bits and `ANG_ZERO_L[7:0]` is the lower 8 bits.

Read-Modify-Write: Register write via I²C/SPI is a 16-bit word access. To modify only `angle_zero[7:0]`, first read back the current value of `ANG_ZERO_L` (0x1A), preserve the upper 8-bit RESERVED field, then write back to avoid overwriting factory-protected fields. See **Appendix A** in Chapter 16 for read-modify-write examples (using `0x19`/`0x1C` register words).

11.5 Analog Output Trim Register OUT_TRIM (Address: 0x1B)

Bit Name	Bit	R/W	Default	Description
out_offset	7:0	RW	0x00	Analog output offset trim. 8-bit signed (two's complement), max trim range $\pm$128 LSB, corresponding to $\pm$11.25°
out_gain	15:8	RW	0x08	Analog output gain trim. 8-bit fixed-point Q5.3 format (5 integer bits, 3 fractional bits). Default 8'b0000_1000 (0x08) = 1$\times$ gain

Description:

- **out_offset:** 8-bit two's complement signed value, range $-128 \sim +127$ LSB. Angle trim resolution is approximately $11.25°/128 \approx 0.0879°$/LSB.
- **out_gain:** Q5.3 format gain factor: $G = \frac{\text{out\_gain}}{2^3}$. For example, 0x08 $\rightarrow$ 1.000$\times$, 0x09 $\rightarrow$ 1.125$\times$.

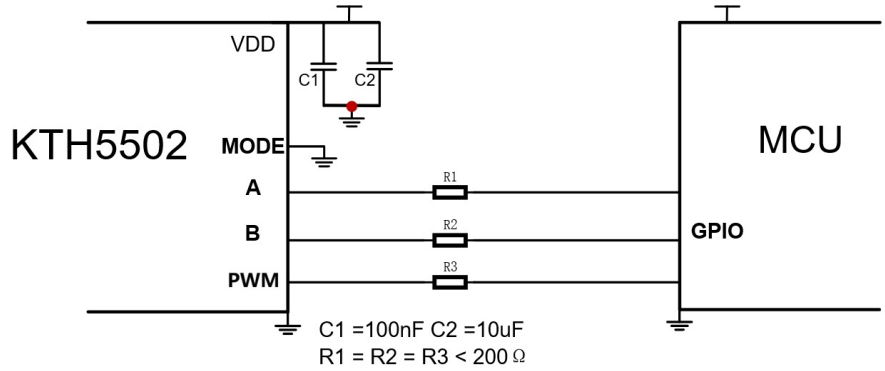
11.6 Digital Filter and CM Mode Configuration Register DIG_FLT (Address: 0x1C)

Bit Name	Bit	R/W	Default	Description
CM_measTime	9:0	RW	0x000	Sets the sleep interval between measurements in CM periodic measurement mode. 0 = continuous measurement; each increment adds 1.25 ms sleep between measurements. Sleep duration formula: T_{sleep} = measTime[9:0] × 1.25 ms. Maximum sleep: 1278.75 ms (1023 × 1.25 ms)
digCtrl	12:10	RW	3'b000	Configures internal digital filtering. Higher values = deeper filtering, longer measurement time
RESERVED	15:13	RO	3'b000	Factory-internal configuration; user modification not allowed

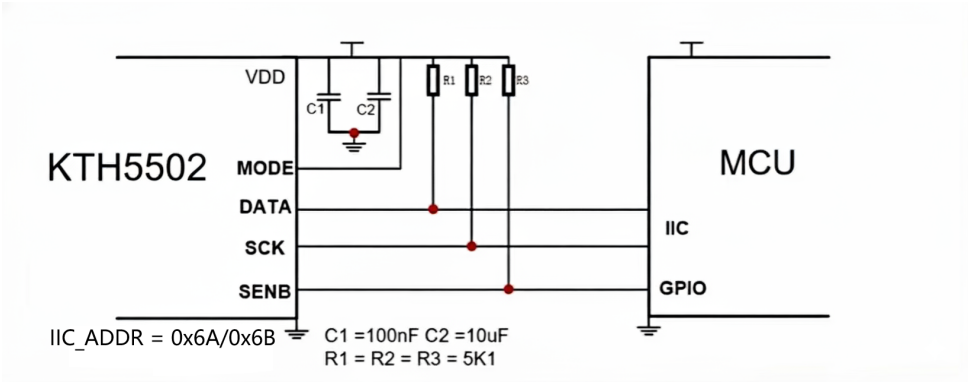
Note: For RESERVED bits, it is recommended to read the current value before writing, modify only the bits to be configured, and then write the complete data back to the register.

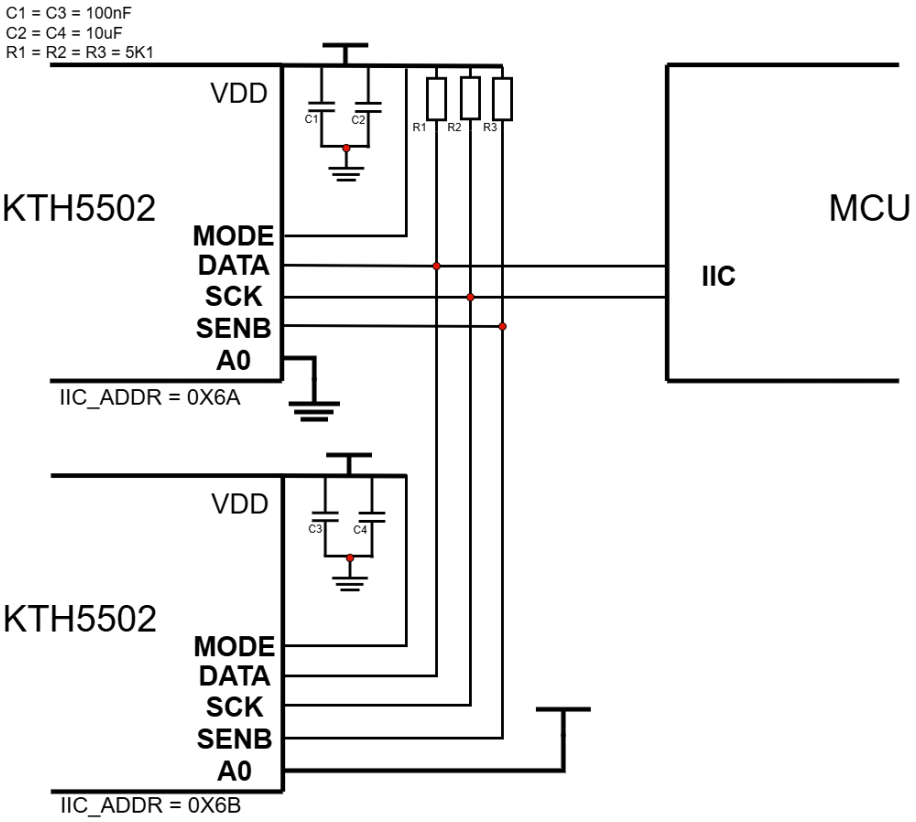
12 Typical Application Circuits

12.1 AB Quadrature Encoding Mode Application Circuit



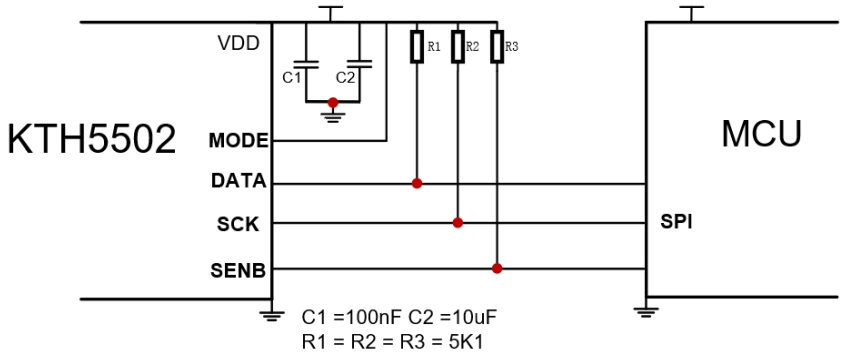
12.2 I²C Mode Application Circuit





Note: When multiple devices share the same I²C bus, the base model can be used, with different address levels applied to OUT/A0 (A0) to distinguish addresses (GND→0x6A, VDD→0x6B). Configure the corresponding slave address in the host driver.

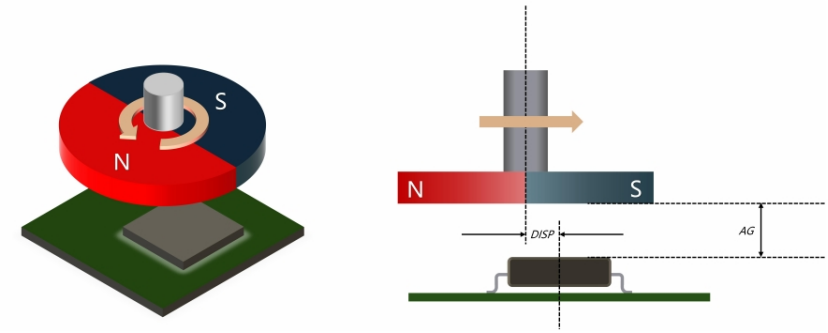
12.3 SPI Mode Application Circuit



13 Magnet Installation Guidelines

To ensure optimal performance of the KTH5502, the following technical specifications should be observed during magnet installation:

Parameter	Specification
Magnet specification	Recommended: 6 mm diameter, 2.5 mm thick, 1-pole-pair diametrically magnetized cylindrical magnet
Air gap	Gap between magnet and chip surface should be 0.5–2.0 mm; recommended 1.0 mm
Alignment accuracy	Offset between magnet center and sensor center should be less than 0.3 mm
Magnetic field strength	Horizontal field component at chip surface should be in the range of 200–1000 Gauss
Interference control	Avoid strong magnetic interference sources such as permanent magnets, inductors, and transformers



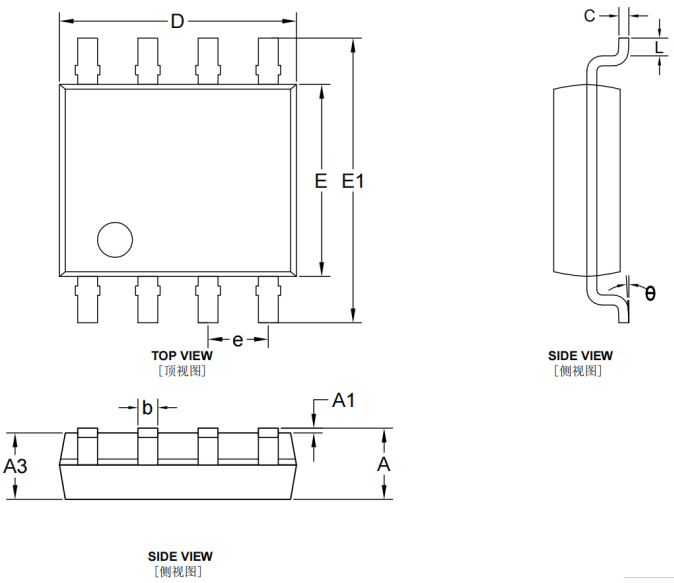
13.1 PCB Layout Guidelines

Tip: Place 0.1μF and 10μF decoupling capacitors between VDD and GND, as close to the chip supply pins as possible.

- Avoid placing strong magnetic interference sources near the sensor
- Minimize copper layers beneath and around the sensor to avoid affecting magnetic field measurements
- Use appropriate decoupling capacitors on power and ground lines, placed as close to the sensor as possible
- Route digital interface traces as far as possible from analog output and sensitive signal paths
- For temperature-sensitive applications, consider thermal design of the sensor to avoid self-heating effects

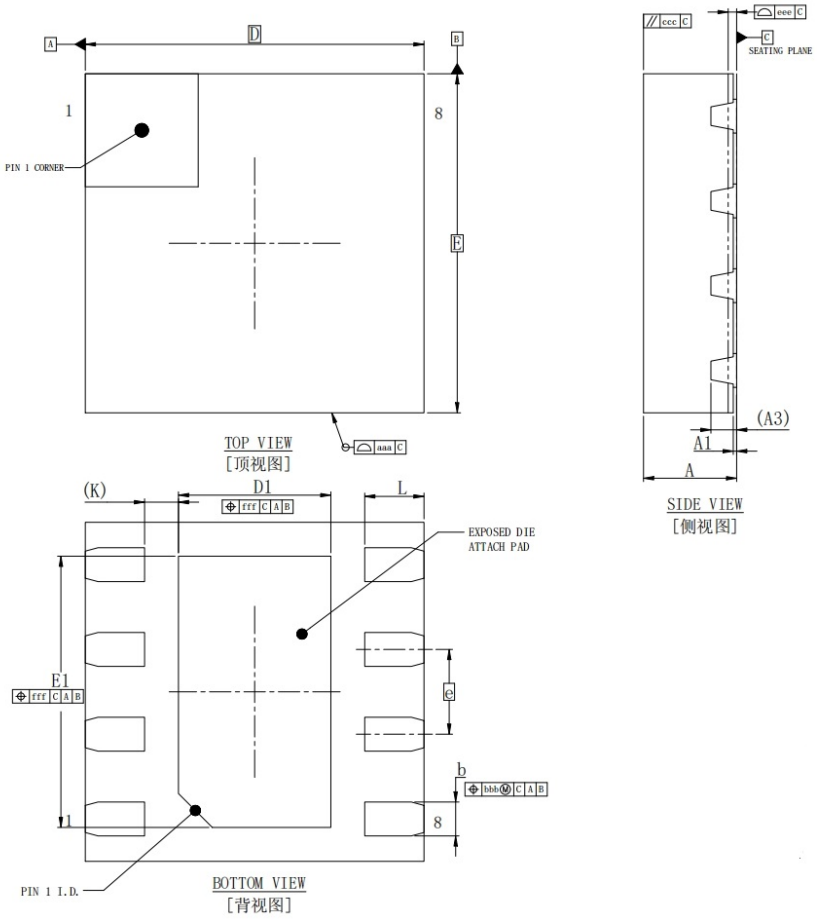
14 Package Information & Mechanical Data

14.1 SOP-8L Package Dimensions



Symbol	Min	Typ	Max	Unit
A	1.350	1.550	1.750	mm
A1	0.100	0.180	0.250	mm
D	4.800	5.000	5.200	mm
E	3.900	4.000	4.100	mm
E1	5.800	6.000	6.200	mm
e	—	1.270BSC	—	mm
b	0.330	0.420	0.510	mm
L	0.400	0.600	0.800	mm

14.2 DFN-8L Package Dimensions



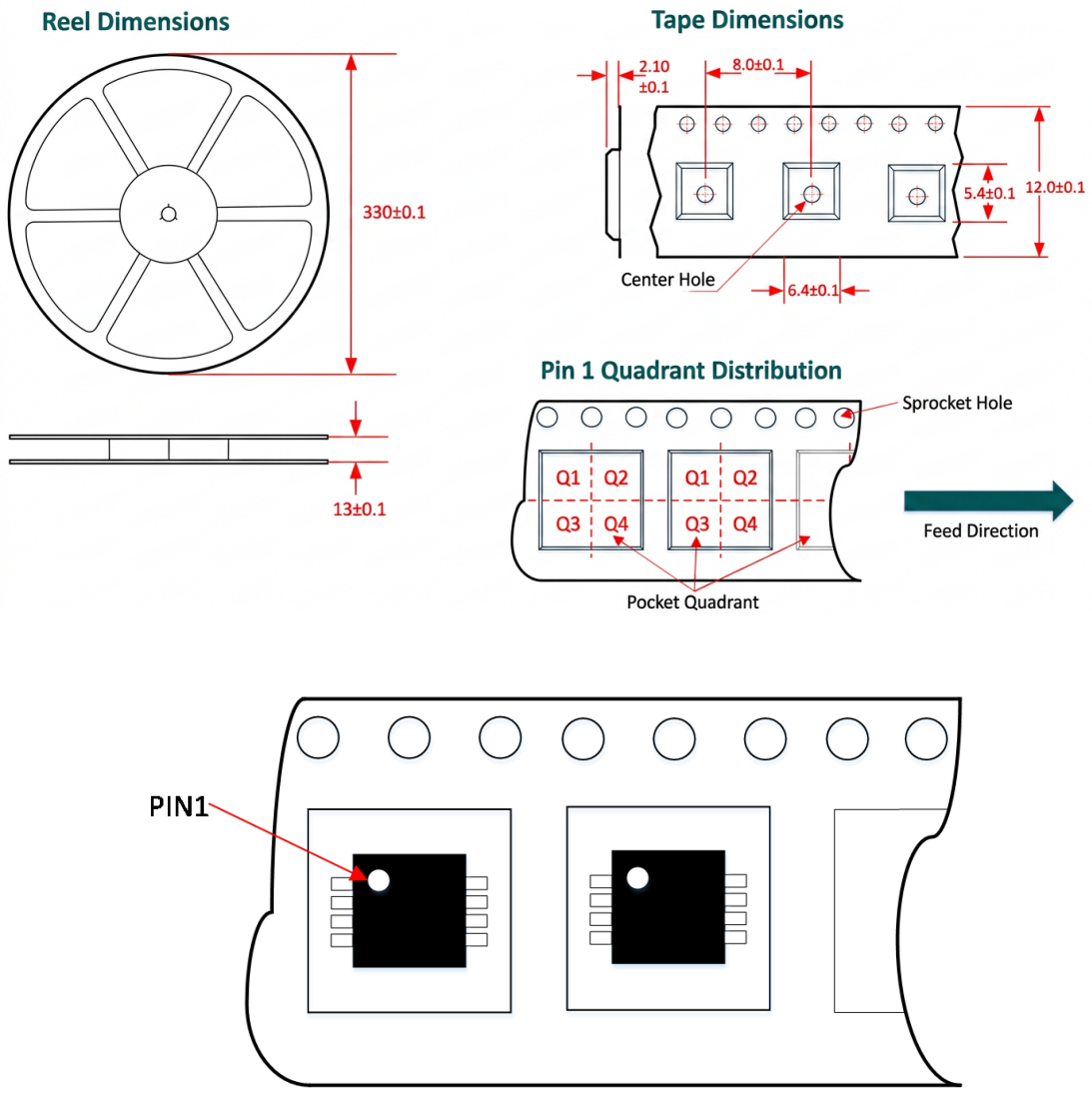
Symbol	Unit: mm		
	Min	Typ	Max
A	0.5	0.55	0.6
A1	0	0.02	0.050
A3	0.152 REF		
D	1.900	—	2.100
E	1.900	—	2.100
D1	0.8	0.9	1
E1	1.5	1.6	1.7
e	0.5 BSC		
b	0.15	0.2	0.250
L	0.3	0.35	0.4
K	0.2 REF		

15 Ordering Information

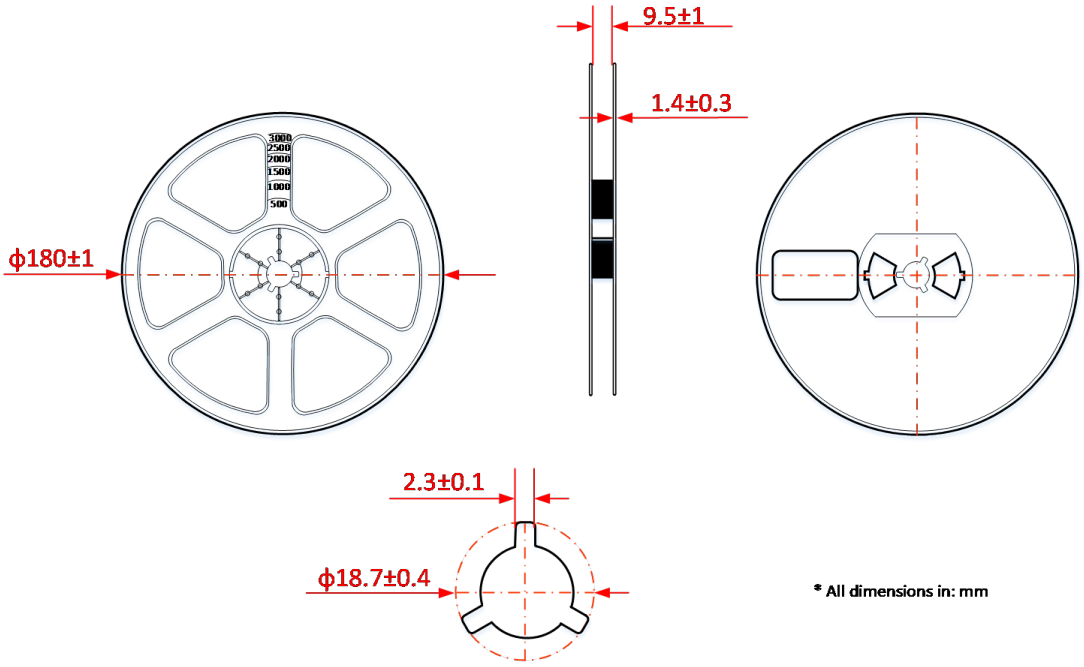
15.1 Product Models

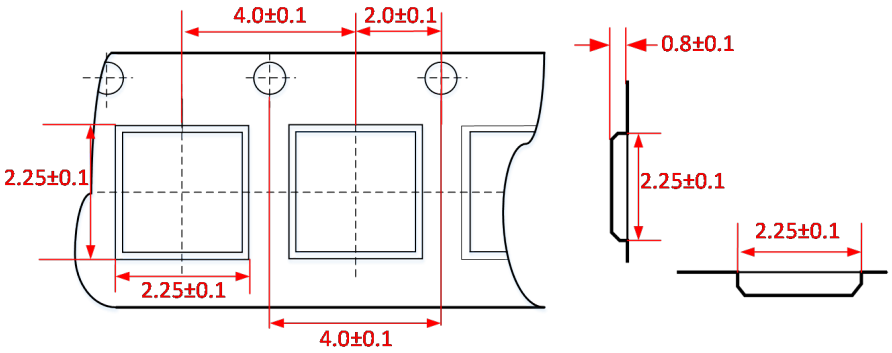
Model	Description	Rec. Speed
KTH5502LVPSP8-AB1024	SOP-8L 1024 lines + analog output + PWM output	≤1000 RPM
KTH5502HVPSP8-AB512	SOP-8L 512 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPSP8-AB256	SOP-8L 256 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPSP8-AB128	SOP-8L 128 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPSP8-AB100	SOP-8L 100 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPSP8-AB50	SOP-8L 50 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPSP8	SOP-8L Base model, 12 lines + I²C address pin (A0) + PWM output	≤5000 RPM
KTH5502LVPDN8-AB1024	DFN-8L 1024 lines + analog output + PWM output	≤1000 RPM
KTH5502HVPDN8-AB512	DFN-8L 512 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPDN8-AB256	DFN-8L 256 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPDN8-AB128	DFN-8L 128 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPDN8-AB100	DFN-8L 100 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPDN8-AB50	DFN-8L 50 lines + analog output + PWM output	≤5000 RPM
KTH5502HVPDN8	DFN-8L Base model, 12 lines + I²C address pin (A0) + PWM output	≤5000 RPM

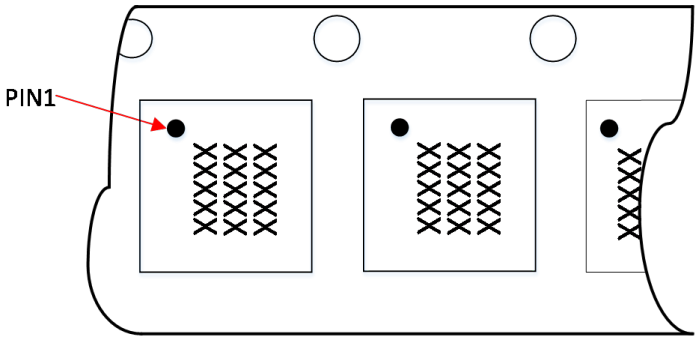
15.2 SOP8 Packaging Information



15.3 DFN-8L Packaging Information (DFN2×2-8L)







16 Appendix

Appendix A: Register Read-Modify-Write Operation Examples

A.1 Applicable Scenarios

When a 16-bit register contains **configuration bits to be modified** along with **read-only/factory-reserved bits** or **other bit fields not intended to be changed**, and the interface protocol requires **16-bit word** writes, the host should first **read back the current word**, merge with a bitmask in software, and then **write back the complete word**. Do not write fixed constants without reading back first, as this may overwrite read-only or reserved fields, or unintentionally modify unrelated bit fields.

A.2 C Reference Code (Modifying pwmFreq in 0x19 / OSR_CFG)

The following example assumes `i2c_read16(reg, *pval)` and `i2c_write16(reg, val)` are available, performing 16-bit read and write at the specified register address (address is the register address byte from the datasheet; specific encoding depends on the host driver implementation). This example corresponds to register `OSR_CFG` (**0x19**, see 11.3): only modifying `pwmFreq` (bit 13), while preserving `magnOsr[15:14]` and `RESERVED[12:0]` from the readback value.

```
#define REG_OSR_CFG 0x19u
#define PWMFREQ_SHIFT 13
#define PWMFREQ_MASK (1u << PWMFREQ_SHIFT)

/* pwm_freq: 0 -> 972Hz(13bit); 1 -> 486Hz(14bit) */
int kth5502_rmw_osr_cfg_pwmfreq(unsigned int pwm_freq_0_or_1)
{
    uint16_t reg;

    if (i2c_read16(REG_OSR_CFG, &reg) != 0)
        return -1;

    reg = (reg & ~PWMFREQ_MASK)
        | (((uint16_t)(pwm_freq_0_or_1 & 1u)) << PWMFREQ_SHIFT);

    return i2c_write16(REG_OSR_CFG, reg);
}
```

A.3 Cross-Bitfield Write (Modifying digCtrl in 0x1C / DIG_FLT)

When the target field is not byte-aligned, the same approach applies: **read back → clear bits by mask → OR in new value → write back word**. The following example corresponds to `DIG_FLT` (**0x1C**, see 11.6): only updating `digCtrl[12:10]`, while preserving `CM_measTime[9:0]` and `RESERVED[15:13]` from the readback value; `dig_ctrl_val` ranges from 0–7.

```
#define REG_DIG_FLT 0x1Cu
#define DIGCTRL_SHIFT 10
#define DIGCTRL_MASK (0x7u << DIGCTRL_SHIFT) /* digCtrl is 3 bits */

int kth5502_rmw_dig_flt_digctrl(unsigned int dig_ctrl_val_0_to_7)
{
    uint16_t reg;

    if (i2c_read16(REG_DIG_FLT, &reg) != 0)
        return -1;

    reg = (reg & ~DIGCTRL_MASK)
        | (((uint16_t)(dig_ctrl_val_0_to_7 & 7u)) << DIGCTRL_SHIFT);

    return i2c_write16(REG_DIG_FLT, reg);
}
```

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